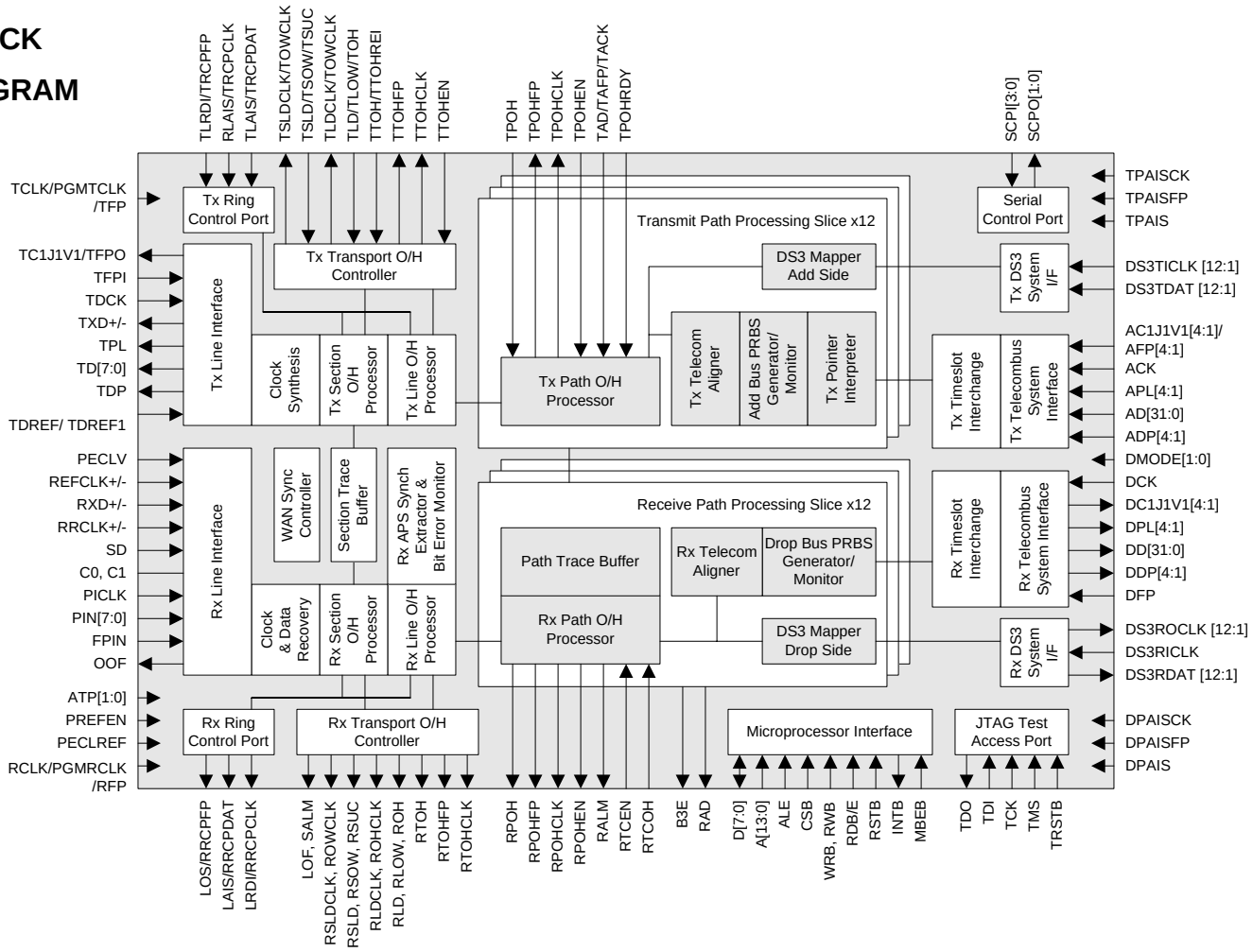
SONET/SDH Payload Extractor/Aligner for 622 Mbit/s Interfaces

FEATURES

The SPECTRA-622 chip offers the following features:

- Monolithic SONET/SDH Payload-Extractor/Aligner for use in STS-12 (STM-4/AU3 or STM-4/AU4) or STM-12c (STM-4/AU4-4c) interface applications that operate at serial interface speeds up to 622.08 Mbit/s.
- Provides integrated clock recovery and clock synthesis to allow a direct interface to optical modules.
- Complies with Bellcore GR-253-CORE jitter tolerance and intrinsic jitter criteria.
- Provides control circuitry required to comply with WAN clocking requirements for wander, holdover, and long term stability.
- Provides termination for SONET Section and Line, and SDH Regenerator Section and Multiplexer Section transport-overhead. Also provides termination for Path overhead of twelve STS-1 (STM-0/AU3) paths, four STS-3/3c (STM-1/AU3/AU4) paths, or a single STS-12c (STM-4/AU4-4c) path.
- Maps twelve STS-1 (STM-0/AU3) payloads, four STS-3/3c (STM-1/AU3/AU4) payloads, or a single STS-12c (STM-4/AU4-4c) payload to system timing references. This accommodates plesiochronous timing offsets between the references.
- Maps twelve DS3 bit-streams into an STS-12 (STM-4/AU3) frame.
- Configurable on an STS-1 basis to support a mix of traffic from the DS-3 and Telecom interfaces.
- Provides a Time-Slot Interchange (TSI) function on the Telecom Add and Drop buses for grooming twelve STS-1 (STM-0/AU3) paths or four STS-3/3c (STM-1/AU3/AU4) paths.
- Supports line loopback and diagnostic loopback.
- Supports OC-48 (STM-16) applications with byte interfaces for connection to an OC-48 front-end device.
- Supports diagnostic 2^{23}-1 pseudo-random bit-sequence (PRBS) generation and monitoring.
- Provides a standard JTAG test-port for boundary scan board-test purposes.
- Provides a generic 8-bit microprocessor bus-interface.
- Low-power 3.3V CMOS with TTL compatible inputs and CMOS/TTL digital outputs. PECL inputs and outputs are 3.3V and 5V compatible.
- Available in a 520-pin SBGA package.
- Supports industrial temperature-range (-40°C to 85°C) operation.

BLOCK DIAGRAM



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BACKPLANE/DEVICE MODES

- 77.76 MHz Telecom Byte
- 19.44 MHz Telecom Byte x 4
- Datacom DS-3 x 12

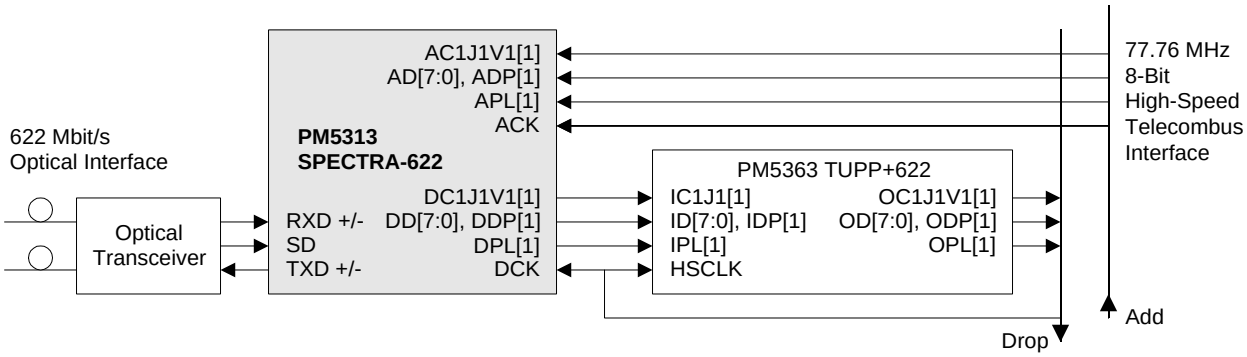
APPLICATIONS

Use the SPECTRA-622 chip in the following applications:

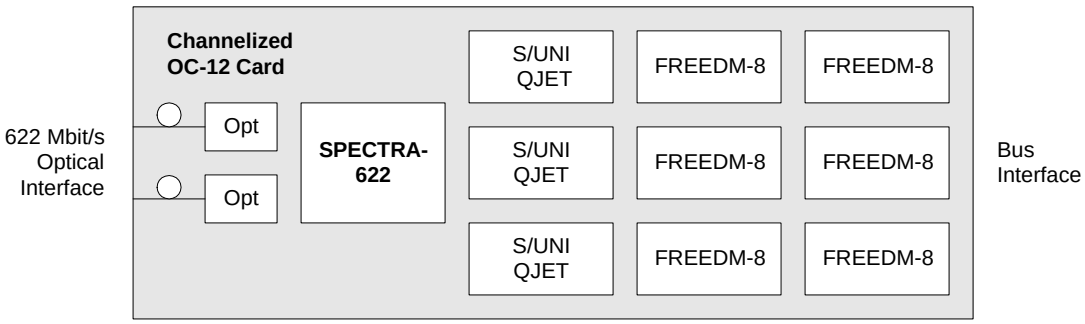
- SONET/SDH Add/Drop Multiplexers
- SONET/SDH Terminal Multiplexers
- SONET/SDH Digital Cross-Connects
- Channelized Routers and Switches

TYPICAL APPLICATIONS

STS-12/STM-4 AGGREGATE INTERFACE WITH TRIBUTARY POINTER PROCESSING AND PERFORMANCE MONITORING



CHANNELIZED OC-12 INTERFACE FOR HIGH SPEED ROUTERS



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